A 1.9 GHZ FULLY INTEGRATED PHS POWER AMPLIFIER WITH A NOVEL AUTOMATIC GATE-BIAS CONTROL CIRCUIT

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Abstract:

A 3.6V PHS power amplifier (PA) GaAs MMIC with on-chip matching circuits *and a novel automatic gate-bias control circuit* is reported. It obviates the need for cumbersome and expensive post fabrication dc bias current tuning. The 1.02x1.73 mm^2 SSOP-16 plastic packaged chip, meets all PHS specifications, and the performance is comparable to the PA without the bias control circuit. The measured PA performance is presented for deep, shallow and typical pinch-off voltage cases confirming the robustness and suitability of the proposed bias control circuit.

Introduction and Key Features:

The reported GaAs MESFET Personal Handyphone System (PHS) PAs [1-8] have not so far fully integrated all the components such as all parts of the matching circuit and/or the automatic gate bias control circuit on the same chip. In some cases special processes with low knee voltage and very high Q inductances have been used [4] to improve the efficiency. Also in a recent publication [1] a two-chip single-package approach has been adopted; the output matching chip being separate from the main PA chip. Further, no PHS PA has been reported to our knowledge which includes an automatic gate-bias stabilization circuit on the same chip. Such a bias current stabilization circuit obviates the need for the cumbersome and time consuming external tuning of the dc bias current after the fabrication which would otherwise be required to counteract for the lot-to-lot variations of the pinch-off voltage (V_p) of the MESFETs. In [5] a negative voltage generator is included however the gate-bias control circuit has not been integrated. *In this paper we present a design which incorporates a novel automatic gate-bias control circuit and on-chip matching circuits, making it the first fully integrated PHS PA to our knowledge.*

While monolithically integrating input, interstage and output matching circuits, chokes, coupling capacitors and even the automatic gate bias control circuit, a very small chip size of 1.02x1.73 mm^2, is achieved due to a relatively dense layout approach adopted as shown in the chip microphotograph, Fig. 1. The chip size is thus one of the smallest reported for PHS application [1-3,5-8].

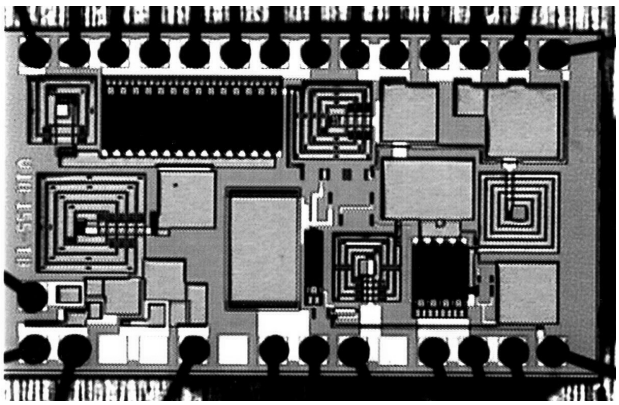

Fig. 1 Chip Microphotograph of the Two Stage PA with Automatic Gate-Bias Control Circuit.

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The chip employs a low cost 1.0 μm recess gate ion-implanted standard MESFET process with three levels of interconnects. The typical supply voltage is 3.6 V; the range is from 3.3-3.9 V. The chip is mounted in a 16-pin SSOP plastic package. It meets all PHS specifications including output power, adjacent channel power (ACP) and harmonics.

The proposed gate bias control circuit stabilizes the bias current with respect to the (i) Vp (ii) VDD and VGG of the bias circuit, and (iii) the variations of resistances employed in the control circuit.

PA Design Considerations and Performance:

The PA schematic, without the automatic bias control circuit, is shown in Fig. 2. Both the stages operate at about 10% IDSS bias point so that one automatic gate bias control circuit could be employed for both the stages. At certain locations, parasitics such as bond-wires and package leads are used to our advantage e.g. the chokes are partly on chip and partly realized using bond-wire and lead inductances. Similarly at the output side the package 'parasitics' helped to obtain a very good harmonic performance. The harmonic performance of the PA is thus better than that of the recently reported circuit [2] which uses a special output matching circuit technique to improve the harmonics. The second and third harmonics of the PA (Table 1) are about 10 to 20 dB better than those reported in [2].

To improve the predictability of the designs, effects of resonance and loss factors of the inductors and capacitors and additional parasitics due to the wide geometry FETs were taken into consideration. Layout precautions were taken to achieve a dense layout to reduce the chip size and to minimize the losses in the interconnects.

Seven bond-wires from the final stage `source' to the die-pad and three bond wires from the driver stage 'source' were employed to minimize the loss in gain. Root model was employed and harmonic balance technique was used for simulations. Simulations at layout level were also performed.

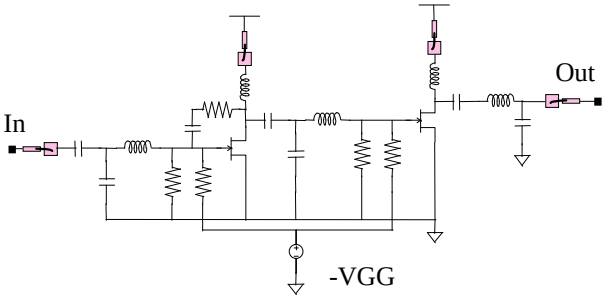

Fig. 2 The Two Stage Power Amplifier Schematic.

Table 1 Typical Measured Performance of the PA (without automatic gate bias control circuit).

Ids (1st / 2nd stage)	35 / 120	mA
Gain	19.9	dB
flatness with Frequency	0.09	dB
flatness with VDD	0.03	dB
PO1	21.5	dBm
flatness with Frequency	0.19	dBm
Variation with VDD	0.38	dBm
PO @ ACPR= - 55dBc	23.0	dBm
ACPR	-56.5	dBc
IP3	33.1	dBm
S11	16.0	dB
S22	7.4	dB
2nd Harmonic	-56.7	dBc
3rd Harmonic	-70.7	dBc
4th Harmonic	-52.7	dBc
Spurious	-80	dBc

As shown in Table 1, measured Gain and 1 dB compression power (PO1) are about 20 dB and 21.5 dBm respectively at a total current of about 155 mA. Since adjacent channel power ratio (ACPR) is better than – 55 dBc at PO1, it is possible to deliver higher power of about 23 dBm, while maintaining the ACPR level of –55 dBc. This also means that the PA is sufficiently linear at more than 2 dB compression. The harmonic performance as mentioned earlier is excellent. The efficiency at 21.5 dBm is about

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24.5% and at higher powers of 22-23 dBm it is about 27-34 %. As seen from Table 1, spurious and gain-flatness etc. are also very good.

The Automatic Gate-Bias Control Circuit:

The proposed gate-bias control circuit is shown in Fig. 3 with its application in the power amplifier circuit that has been discussed above. QB is the only MESFET used for the bias stabilization. The other MESFET QP is for power amplification.

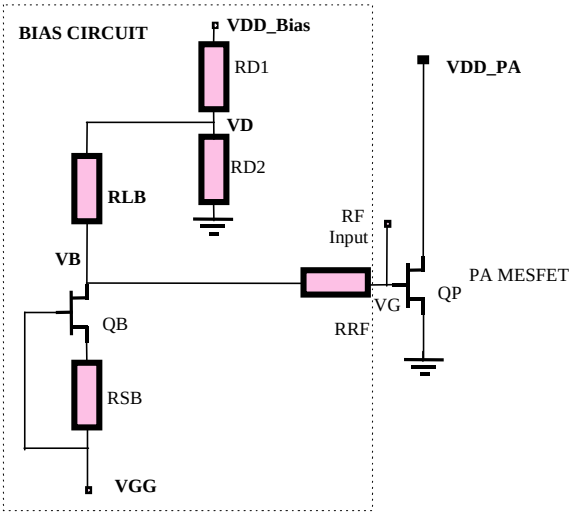

Fig. 3 The Automatic Gate Bias Control Circuit

The basic operation of the circuit is as follows. If Vp is more negative than the nominal, the current would be greater than its nominal value in both the main MESFET QP and the bias control MESFET QB. The increased current in QB would make the voltage VB more negative. This action tends to keep the dc current through QP relatively constant assuming that the Vp's of the two MESFETs are strongly correlated. The gate-width of QB is much smaller than that of the MESFET QP. Resistor RRF is useful to isolate various RF circuits driven by the same bias circuit. Thus we could use just one gate bias control circuit for both stages of the PA. No oscillations were observed.

The proposed bias control circuit stabilizes the dc bias current through the FETs of the PA not only with respect to Vp but with respect to VDD_Bias, VGG and resistor variations as well. This is achieved by the novel circuit configuration as shown in Fig. 3 and by having VGG = - VDD_Bias. To achieve stabilization with respect to resistor variations, a part of the load, namely the resistors RD1 and RD2, was kept external to the chip. It is not always essential but it helps to improve the performance.

The simulated dc bias stabilization performance of the automatic gate bias control circuit is shown in Table 2 with respect to the various factors discussed above assuming that the Vp's of the two MESFETs are exactly equal. EEFET3 model was used for simulations. Table 2 indicates an excellent bias-stabilization performance (-6% to +17 %) with respect to the four variables considered. Thus the proposed bias current stabilization circuit would obviate the need for the time consuming external tuning after the fabrication.

The bias circuit itself carries a very small current of about 2.6 mA making it suitable for working with inverter circuits. Still the ouput resistance seen by the leakage current of the main MESFET QP is low enough that no thermal runaway problem was encountered during the measurements.

Table 2 Simulation Results of Automatic Gate Bias Control Circuit

Bias Transistor Current : ~ 2.6 mA		
Parameter	***Parameter Variations***	***% Ids Variation***
Vp	-2.2V / -2.9V	-6.0 / 17.1
VGG (=-VDD_Bias)	3.3V / 3.9V	-5.2 / 16.7
Internal R	+/- 20%	-1.0 / 0.9
External R	+/- 1%	4.7 / -4.6

Table 3 shows the measured data from the fully integrated PA MMICs (PA with the automatic bias control circuit) for which the Vp was intentionally varied. Data from 'typical', 'shallow' and `deep' Vp chips is tabulated. The

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average idle current in the Vp varied chips is within -2.6 / +7 % for the first stage and within +2.5 / 8.6 % for the second stage. It is also evident from Table 3 that the PA performance for gain, PO1 and ACP is comparable to that of the PA without the bias control circuit (Table 1). About 1.5 dB smaller gain is observed which is partly due to the differences in the bonding configurations. The total idle current is higher due to the systematic mismatch in the Vp of the big PA FETs and the small bias control FET. It can be corrected easily by having different external RD1 or RD2 values. This is needed as a 'one time correction' to take care of the systematic offset in Vp's and no correction for lot to lot variations would be needed thereafter.

To conclude, the proposed automatic gate-bias control circuit meets the most important objective of avoiding the cumbersome and expensive post fabrication tuning of the dc bias current which would otherwise be required to counteract for the lot-to-lot variations of the Vp of the MESFETs. It is clear from Table 3 that measured idle current, gain, PO1 and ACP track quite well in spite of a big variation of about 0.5 V in the Vp of the devices.

Conclusions:

A 3.6V PHS GaAs MMIC PA with on-chip matching circuits *and a novel automatic gate-bias control circuit* is reported. It obviates the need for cumbersome post fabrication dc bias current tuning. The 1.02x1.73 mm^2 SSOP-16 plastic packaged chip, meets all PHS specifications. The measured idle current, gain, PO1 and ACP track quite well in spite of a big variation of about 0.5 V in the Vp of the devices.

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Table 3 Measured Results of Two Stage PA with Automatic Gate Bias Control Circuit

V_p Case	V_p (Average) V	IDS - 1st Stage I_{idle} /@ 21.5dBm mA →	ΔI_{idle} wrt Typ. %	IDS - 2nd Stage I_{idle} /@ 21.5dBm mA →	ΔI_{idle} wrt Typ. %	Gain dB	PO1 dBm	ACPR @PO=21.5 dBm dBc
Deep	-2.73	33.5/37	7	176/162	8.6	17.9	22.2	- 56.4
Typical	-2.49	31.3 /35	0	162/148	0	18.6	21.2	- 58.0
Shallow	-2.21	30.5/33.5	-2.6	166/154	2.5	18.4	21.3	- 56.8

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